What is claimed is:

1. A method, comprising:

providing at least one buffer in a memory interface between a chipset and a plurality of memory modules, each module having a plurality of memory ranks, said at least one buffer allowing the memory interface to be split into first and second sub-interfaces, where the first sub-interface is between the chipset and said at least one buffer, and the second sub-interface is between said at least one buffer and the memory modules, such that said at least one buffer provides electrical isolation between the chipset and the memory modules;

configuring said at least one buffer to latch data being transferred between the chipset and the memory modules, such that the first and second sub-interfaces operate independently but in synchronization with each other; and

interleaving outputs of said at least one buffer.

2. The method of claim 1, wherein interleaving allows bit numbers required on said second sub-interface to double.

3. The method of claim 1, wherein providing at least one buffer isolates the first and second sub-interfaces in such a manner that the first sub-interface is operated at different voltage level than the second sub-interface.

4. The method of claim 3, wherein an operating voltage level of said first sub-interface is less than 1.0 volt.

5. The method of claim 3, wherein an operating voltage level of said second sub-interface is between 1.2 and 1.8 volts.

6. The method of claim 1, wherein providing at least one buffer isolates the first and second sub-interfaces in such a manner that the first sub-interface is operated at a higher frequency than the second sub-interface.

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7. The method of claim 6, wherein said first sub-interface is operated at twice the frequency of the second sub-interface.

8. The method of claim 7, wherein a number of data lines in said first sub-interface is half that of a number of data lines in said second sub-interface.

9. The method of claim 1, wherein interleaving outputs of said at least one buffer is provided by connecting the outputs together in a wired-OR mode, and sequentially reading data from the buffer onto a data bus connected to the chipset.

10. The method of claim 1, wherein interleaving outputs of said at least one buffer is provided by multiplexing the outputs, and sequentially outputting data onto a data bus.

11. The method of claim 1, further comprising:

providing a control logic to coordinate the transfer of data from said at least one buffer in an interleaved mode.

12. The method of claim 1, wherein each of said memory modules includes dynamic random access memory (DRAM).

13. The method of claim 1, wherein each of said memory modules includes double data rate (DDR) DRAM.

14. The method of claim 1, wherein each of said memory modules includes quad data rate (QDR) DRAM.

15. A method, comprising:

isolating a memory interface between a chipset and at least one memory module, each memory module containing a plurality of memory ranks, where isolating divides the memory interface into first and second sub-interfaces;

configuring said first and second sub-interfaces to transfer data between the chipset and said at least one memory module, such that the first and second sub-interfaces operate independently but in synchronization with each other; and

interleaving outputs of said plurality of memory ranks,

where said first and second sub-interfaces are configured in such a manner that the first sub-interface is operated at a different voltage level and at a higher frequency than the second sub-interface.

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16. The method of claim 15, wherein said isolating a memory interface is provided by at least one buffer disposed between said chipset and said at least one memory module.

17. The method of claim 15, wherein an operating voltage level of said first sub-interface is less than 1.0 volt, and an operating voltage level of said second sub-interface is between 1.2 and 1.8 volts.

18. The method of claim 15, wherein said first sub-interface is operated at twice the frequency of the second sub-interface.

19. The method of claim 18, wherein a number of data lines in said first sub-interface is half that of a number of data lines in said second sub-interface.

20. A system, comprising:

a chipset;

at least one memory module, each module including a plurality of memory ranks;

a memory interface between said chipset and said at least one memory module;

at least one buffer disposed in said memory interface to divide said memory interface into first and second sub-interfaces, where said first and second sub-interfaces are configured in such a manner that the first sub-interface is operated at different voltage level and at higher frequency than the second sub-interface, and where multiple outputs of said at least one buffer are interleaved.

21. The system of claim 20, further comprising:

a control logic to sequentially read said interleaved outputs of said at least one buffer onto said memory interface.

22. The system of claim 20, wherein an operating voltage level of said first sub-interface is less than 1.0 volt, and an operating voltage level of said second sub-interface is between 1.2 and 1.8 volts.

23. The system of claim 20, wherein said first sub-interface is operated at twice the frequency of the second sub-interface.

24. The system of claim 23, wherein a number of data lines in said first sub-interface is half that of a number of data lines in said second sub-interface.